

FIGURE 1
PRIOR ART

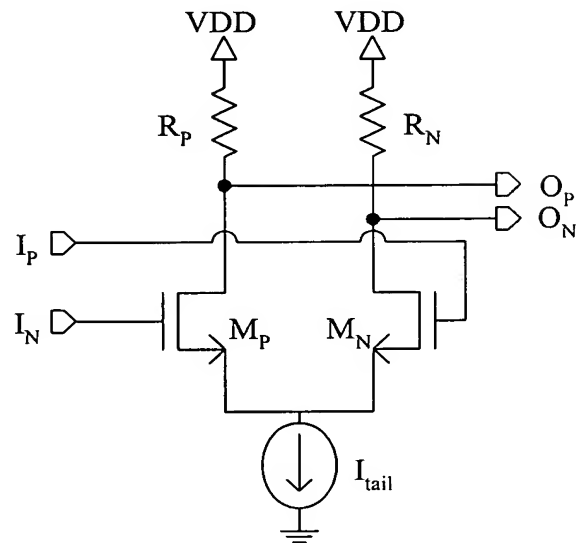


FIGURE 2
PRIOR ART

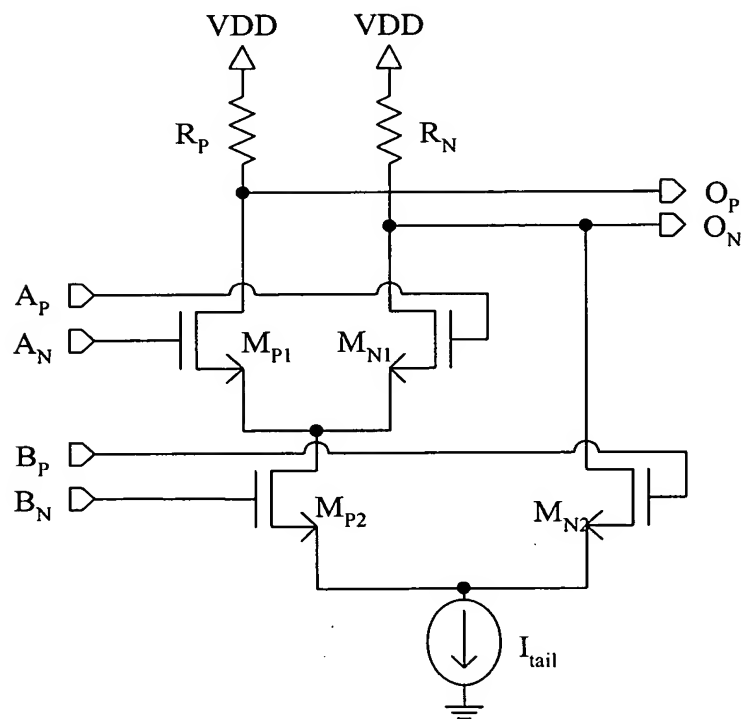


FIGURE 3
PRIOR ART

The diagram shows a differential pair of MOSFETs, M_P and M_N , connected to a common tail current source I_{tail} . The gates of M_P and M_N are driven by differential-mode input signals I_P and I_N . The drains of M_P and M_N are connected to VDD through series combinations of a resistor (R_P , R_N) and an inductor (L_P , L_N). The output signals O_P and O_N are taken from the drain nodes. The inductors L_P and L_N represent parasitic inductances in the signal paths.

Figure 1 consists of two circuit diagrams, 600 and 610, illustrating input impedances. Diagram 600 shows a resistor R in series with a parallel combination of a capacitor C_p and an input impedance Z_{in} . Diagram 610 shows an inductor L in series with a parallel combination of a resistor R , a capacitor C_p , and an input impedance Z_{in} .

FIGURE 6

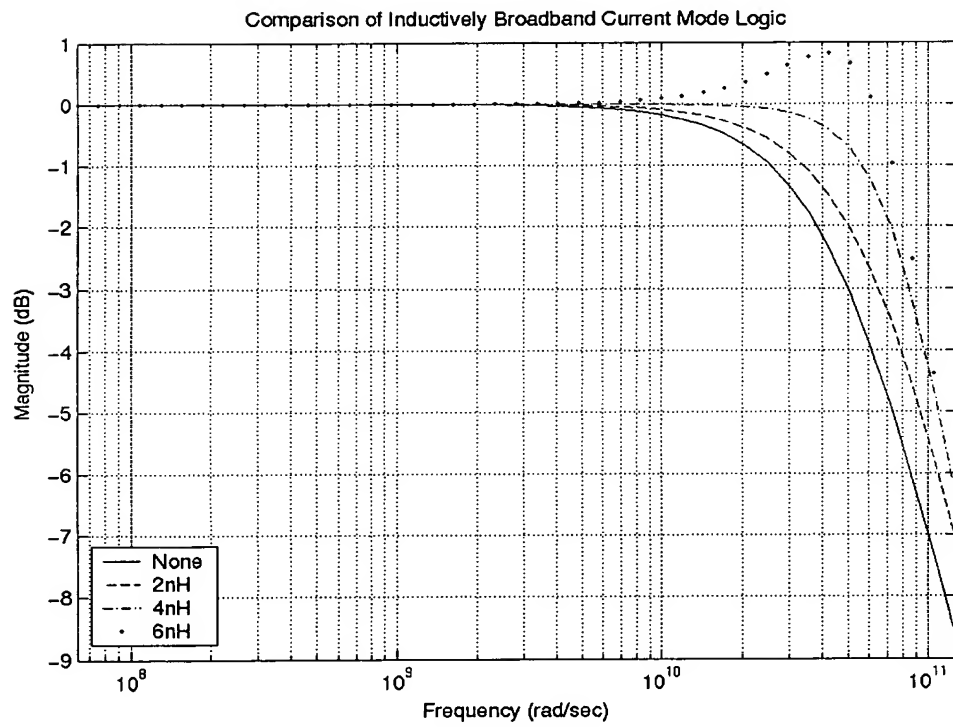


FIGURE 7

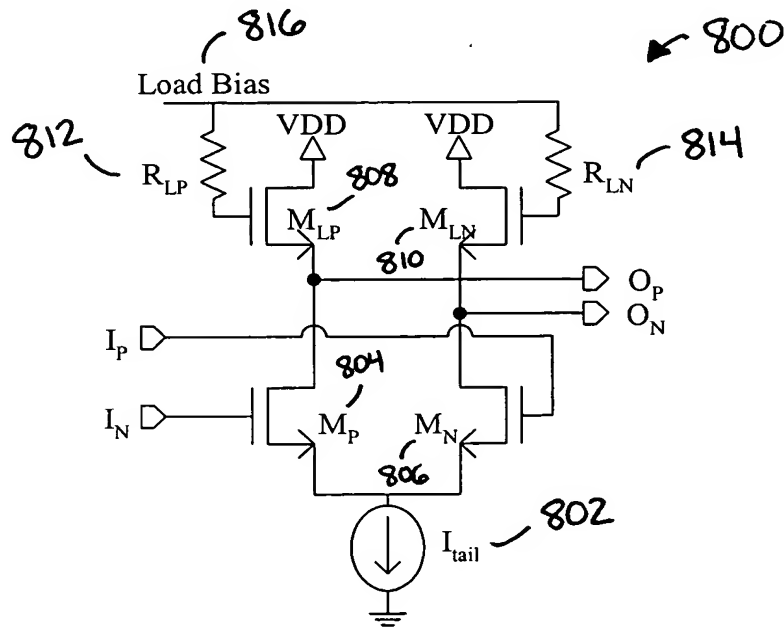


FIGURE 8

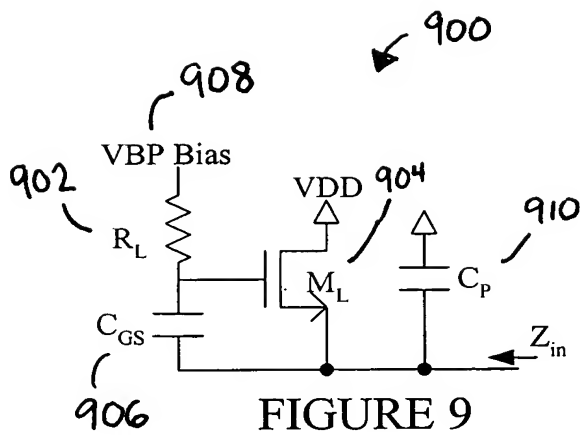


FIGURE 9

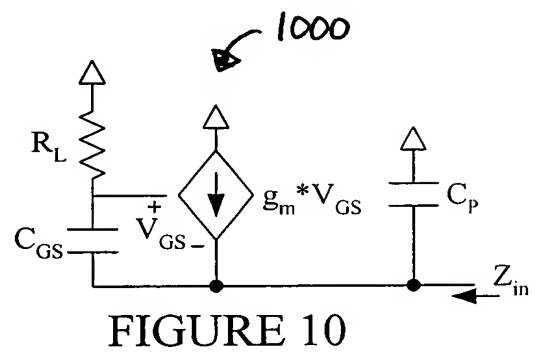


FIGURE 10

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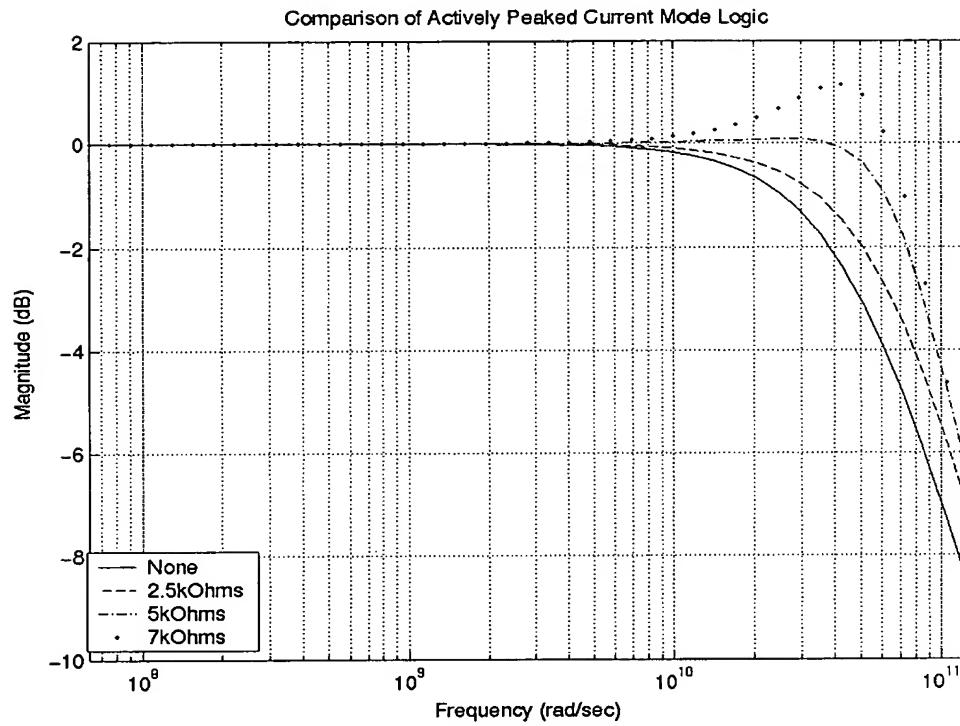


FIGURE 11

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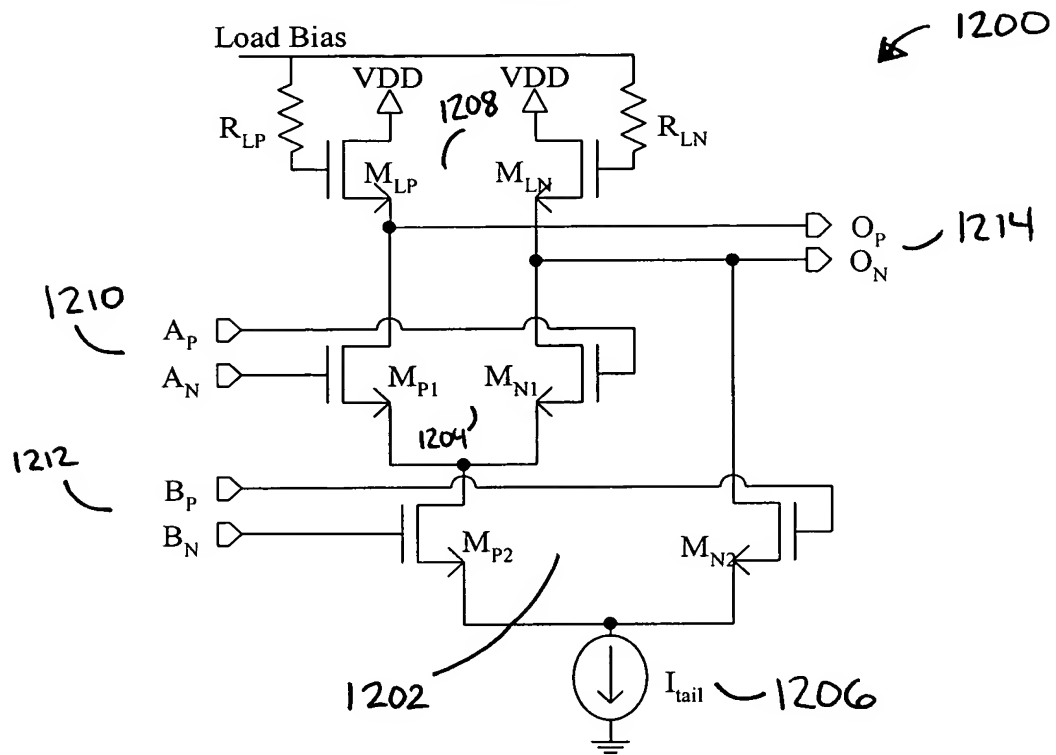


FIGURE 12

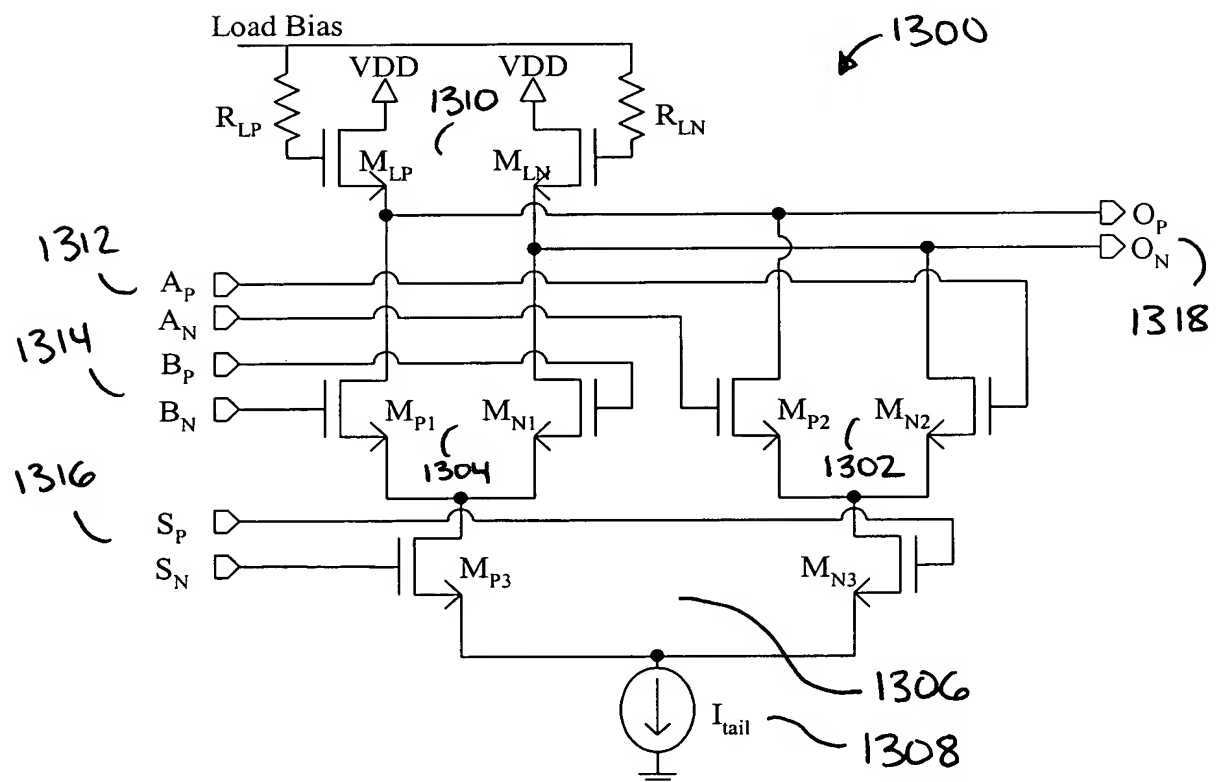


FIGURE 13



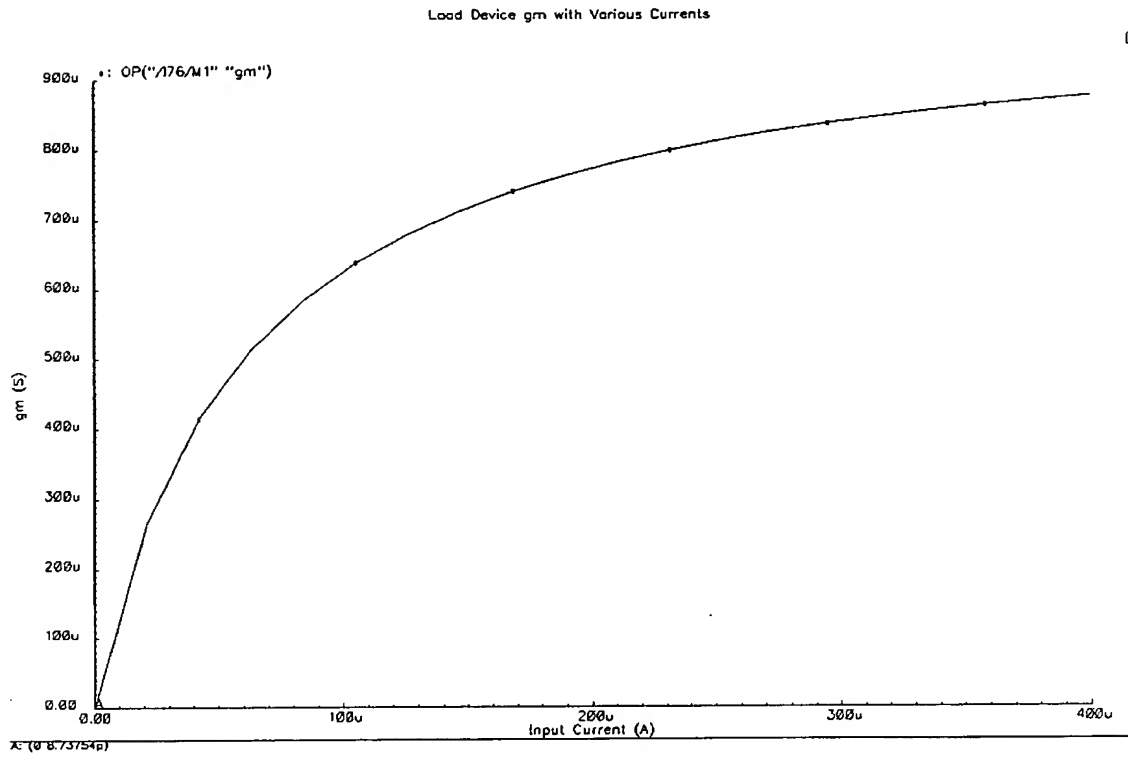


FIGURE 16

FIGURE 17

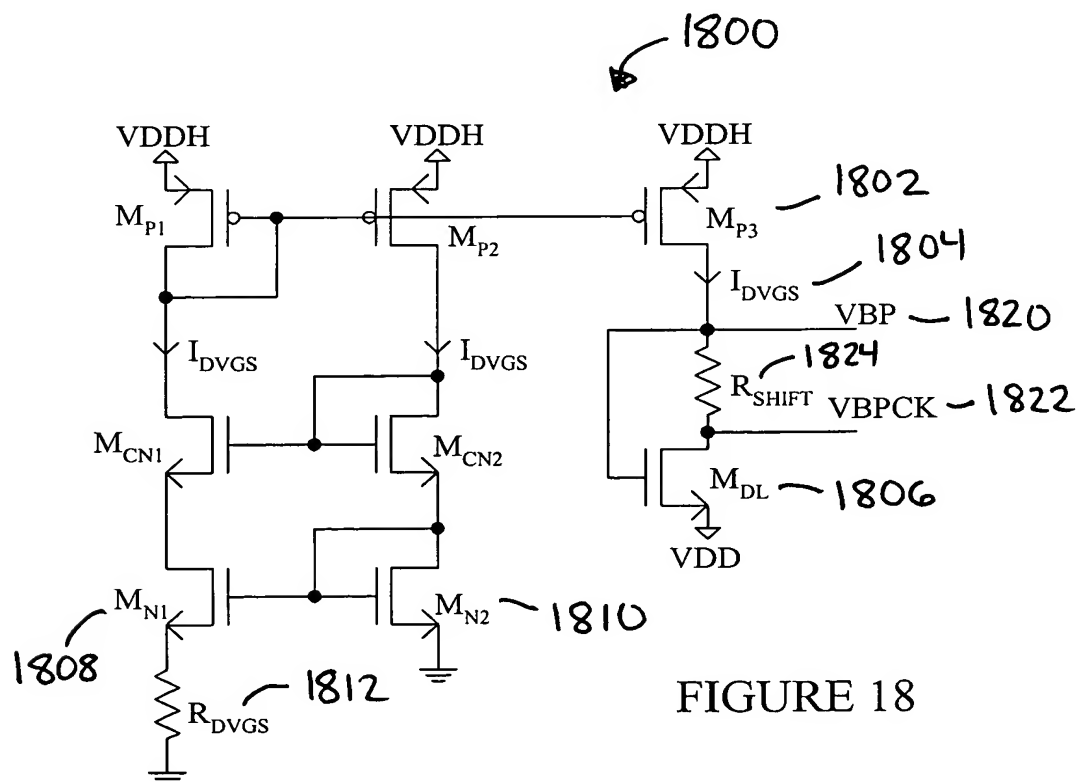


FIGURE 18

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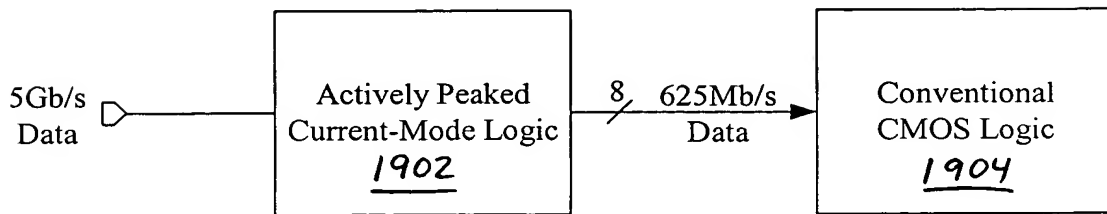


FIGURE 19

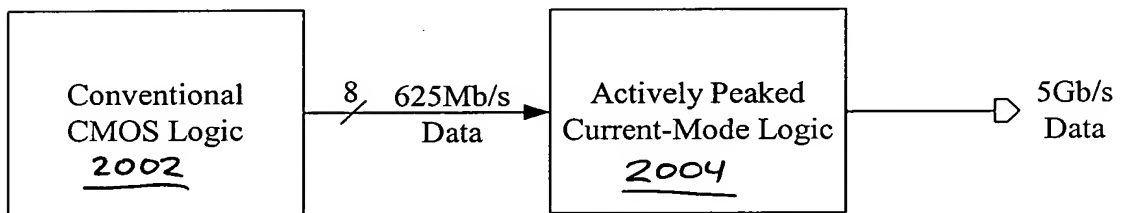


FIGURE 20

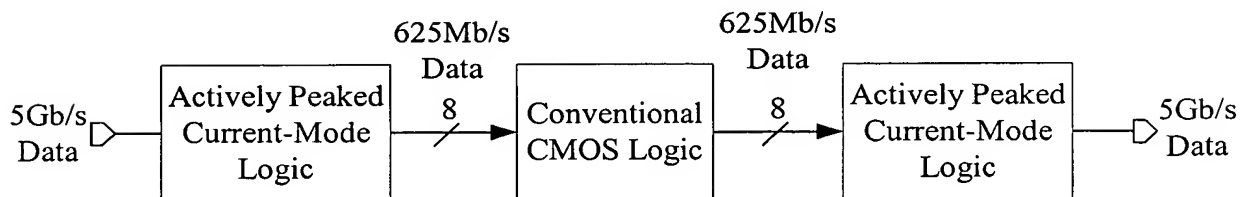
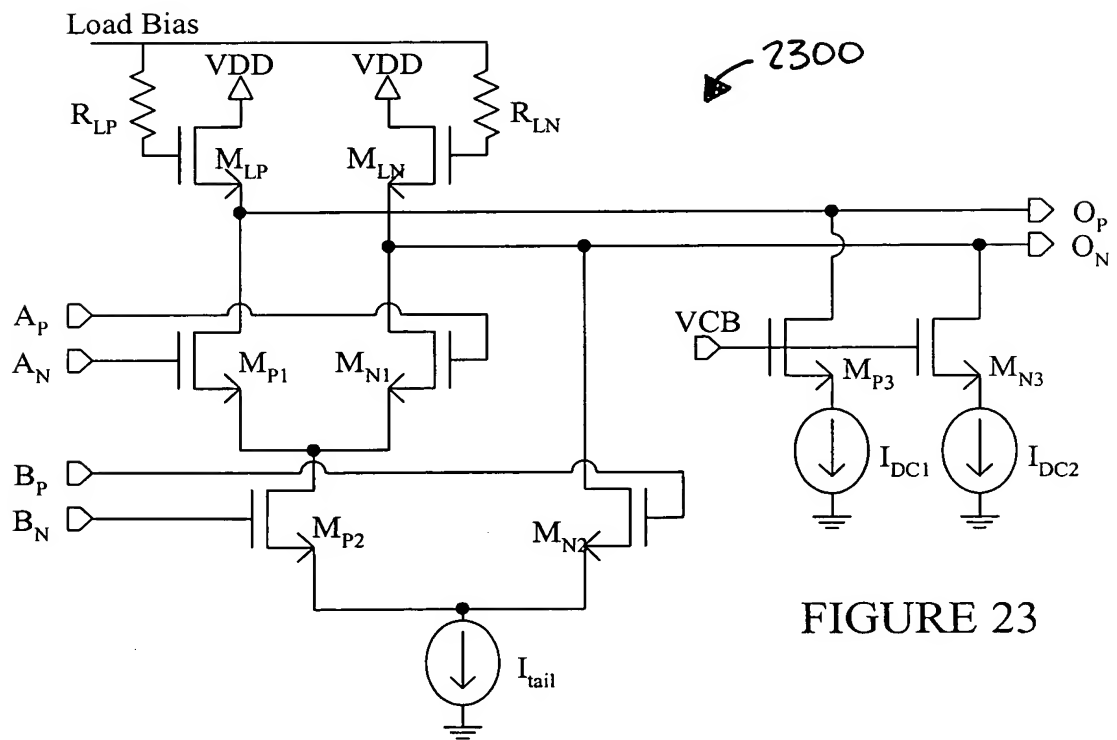
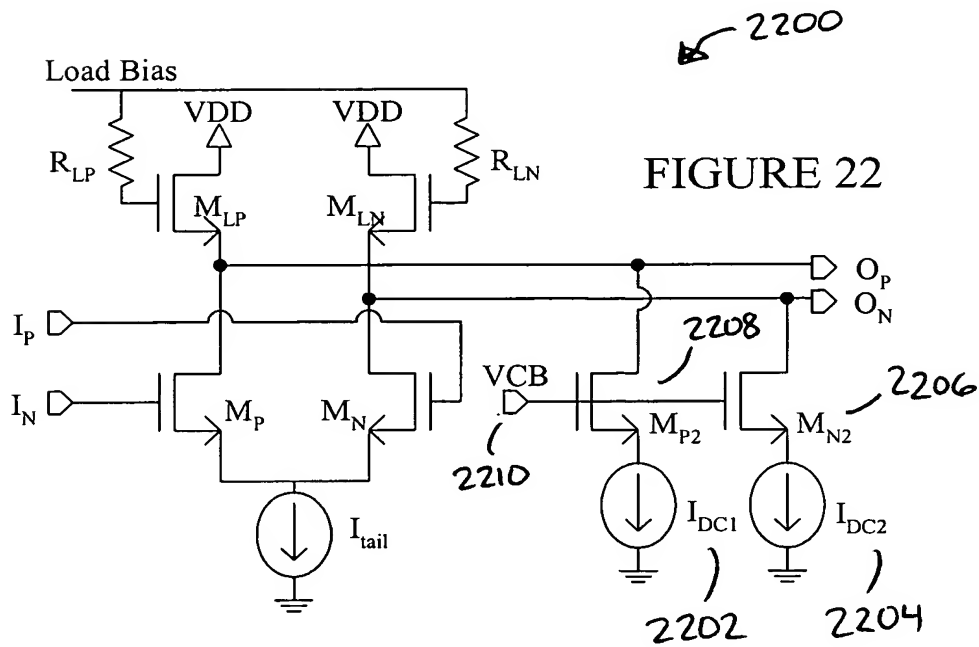
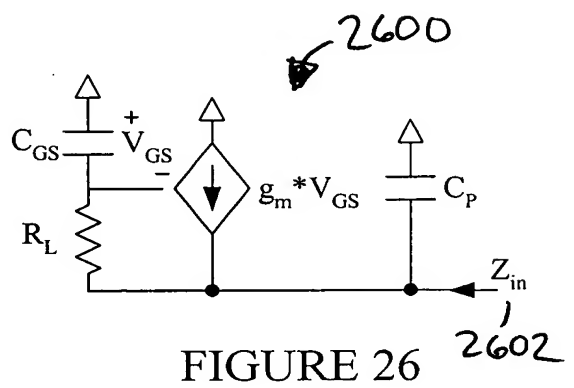
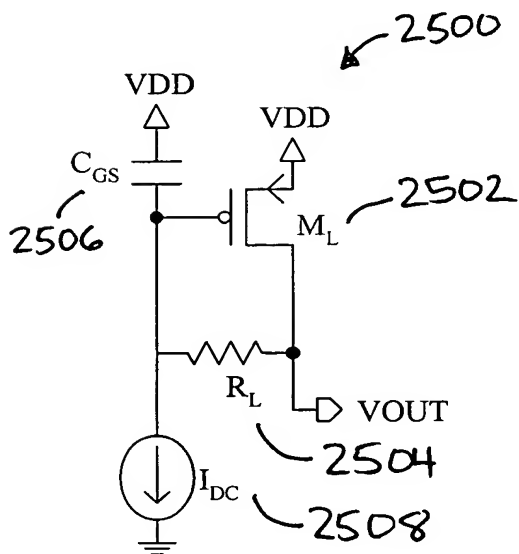
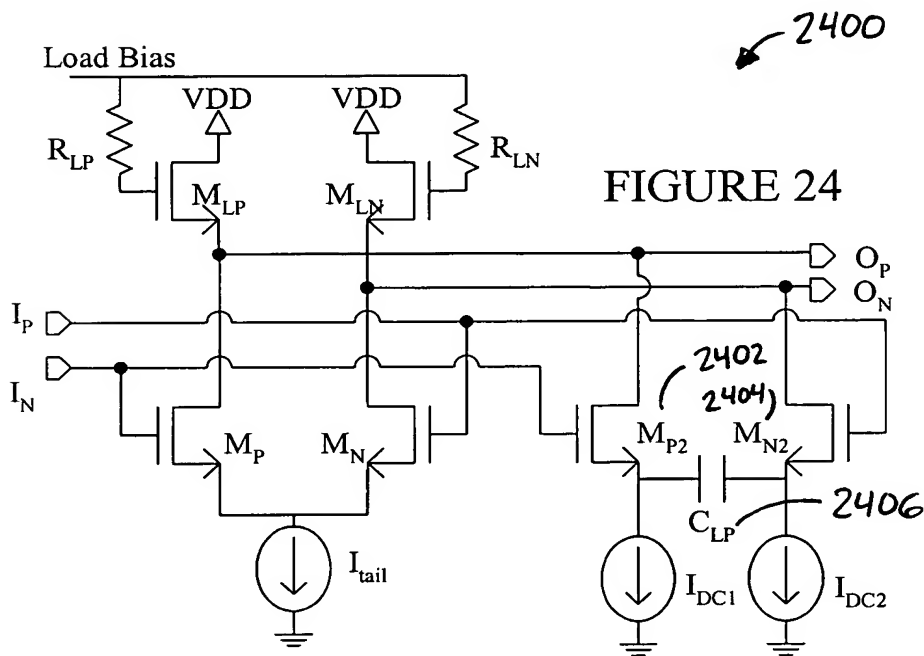


FIGURE 21





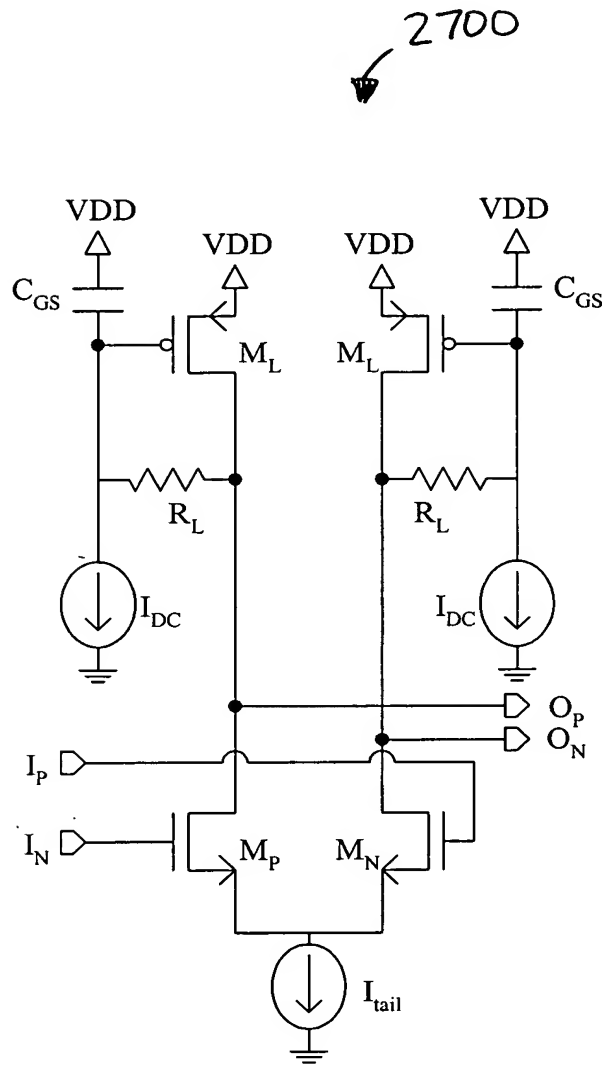


FIGURE 27



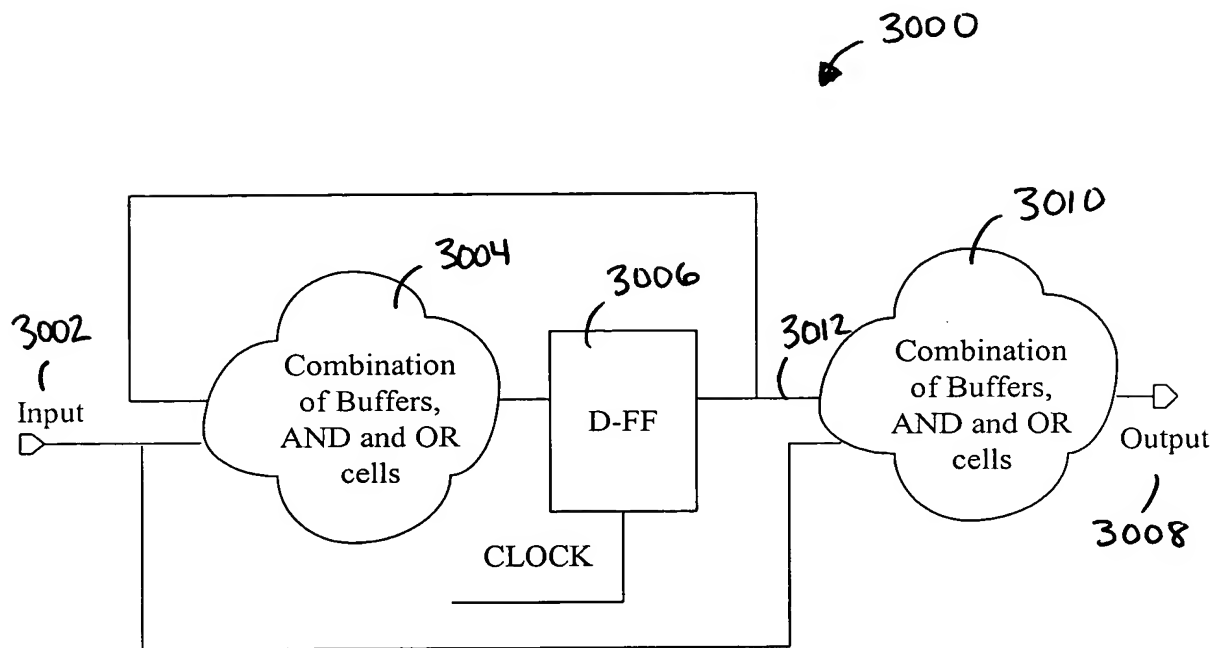


FIGURE 30